DZero Run IIb Production Readiness Review Form

Based on: Version 1.1 (12/02/02)

This document can be found at
http://www.phys.ksu.edu/~evt/PurpleCardPRR.doc

i) Name: Alice Bean, Marcel Demarteau

ii) Date: January 2003

iii) Subsystem: Run IIb Silicon Readout Electronics,

iv) Element(s) being considered for review, including WBS number(s):

The element being considered for review is the so-called 'Purple Card'. This is a card used in the testing and burn-in of all hybrids, modules and staves for the Silicon Detector. The project calls for the production of 75 cards. The WBS number associated with the test card is 1.1.2.14.4. Purple Cards

v) Start/finish dates. Please include brief description: for example, date order is to be placed (where relevant), date production begins/ends, etc.:

The design of the Purple Card started in February of '02. It has undergone one revision. The production order for these cards is for the third version of the card. Production is scheduled to start January 10, '03, for a ten week production cycle. Testing of the cards should commence at the end of March.

a) Scheduled start date/currently anticipated actual start date:

The scheduled start date for the procurement is January 10, '03. The project is ready to place the order as soon as the review is completed.

b) Scheduled finish date/currently anticipated actual finish date:

The scheduled finish date for the production of the boards is March 21, '03. Production is followed by a period of testing and debugging, which is scheduled to be completed on May 5 of '03, (WBS 1.1.2.14.4.8), which indicates the completion of this task.

vi) Cost of WBS element being considered. Please list equipment and labor costs separately, and break out both according to funding type (EQU, In Kind MRI, etc.):

M&S costs: $38,288.0 R&D Funds
FNAL labor cost: $0
A labor cost of $800.00 is part of the M&S cost. The procurement of purple cards is part of the M.O.U. between Kansas State University and Fermilab.

vii) Has element been reviewed previously internal to either the experiment or the Run IIb project? If so, please elaborate. Include extent to which technical approach/scope, cost, and labor needs have been examined, and the conclusions.

The purple card has been reviewed for the first prototype submission. This review was internal to the Silicon Readout Electronics group. The second version of the Purple Card went through a review by email. The proposed changes of the card were limited in scope and the review could be completed by email exchange. The second review received valuable input from the users of the card, notably Yvgeny Zverev. The second version of the Purple card has been successfully used in the readout of many R&D tests for Run 2b electronics and the first prototype modules. A complete list is given in Appendix A. The review of the second version of the Purple Card covered all aspects of the functionality of the card.

As for labor needs and cost, given that the project has produced two prototype versions of this card already, we believe that the estimates for cost, schedule and labor are realistic.

viii) Please include a brief description of the status (and location) of available documentation:

Test results with the purple card have been presented at almost every silicon electronics meeting. Minutes can be found at:
http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/readout/minutes.html
Documentation for the card for the Lehmann review:
http://d0server1.fnal.gov/projects/run2b/Silicon/www/smt2b/readout/purple_card.htm
The Purple Card schematics and layout is documented at KSU:
http://www.phys.ksu.edu/hep/dzero/index.htm
A test manual is also available online:
http://www.phys.ksu.edu/hep/dzero/Purple_card2_8feb02.doc
This test manual will be made available as a D0 note.

ix) Overall recommendation from Subproject (scope, form of review, desired start and completion dates, etc.):

Even though the Purple Card will not be used in the final detector, it plays a critical role in the construction and successful operation of the RunIIb silicon detector. Each and every hybrid, readout module and stave that will find its way in the final detector will be tested with this card. The complete quality assurance of the individual readout components and the grading of the readout parts will be performed with this card. It is therefore of utmost importance that this card functions as specified. Therefore a review is recommended.
The review will be based on the 2nd prototype of the purple card. Since this card has been used successfully already in many tasks, the actual review itself may be rather light. We recommend that a review of two to three hour duration should suffice.

x) Is a Review Committee being recommended? Please state your reasoning, whether pro or con:

A review committee for the Purple Card is recommended. The Purple Card spans many different groups of the Silicon Project. The Testing subgroup of the Silicon Project is the group that will use this card most extensively. Some of the crucial players of the Testing group have not been heavily involved in the discussions for the first two prototype boards. We believe that their feedback is invaluable. Moreover, RunIIa veterans have not really been involved in the design of the card. Again, their participation is strongly desired. As stated above, this card will be used for the quality assurance of each component that will be placed in the detector and therefore prudence calls for a review to ensure that nothing is overlooked and to provide those who will use the card most extensively and opportunity to comment on the design.

xi) If a review Committee is thought to be needed, please include your proposals for each of the following:

a) Committee composition (i.e., internal/external to Project or Laboratory, type and number of personnel, technical expertise required, etc.):

We recommend an internal review committee, with people from just silicon. The panel should consist of someone from Run2a with electronics experience and someone from the testing group, who are the main users of the card. See below for the proposed composition.

b) Committee membership (by name, if known):

Cecilia Gerber (representing the testing group)
Ron Lipton (RunIIa and electronics expertise)
Ron Sidwell
Johnny Green (general card fabrication)

Kazu Hanagaki (member at large)
Sara Lager (member at large)

In addition, the L2 and L3 electronics project managers should be present and Rusell Taylor or Tim Sobering who are the designers of the card.

c) Explicit charge to committee:
Review the layout and functionality of the proposed Purple Card to ensure that it meets all the requirements for the testing of hybrids, modules and staves for the RunIIb silicon detector.

d) Review outline or agenda:
N/A

e) Start date and length of review:
We should try to get this review done in the month of January 2003.
Review should take 2-3 hours at most.

Signatures:

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Level 3 Subproject Manager 1 Date

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Level 3 Subproject Manager 2 Date

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Level 2 Subproject Manager 1 Date

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Level 2 Subproject Manager 2 Date

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Associate Project Manager Date

_____

Deputy Project Manager Date

_____

Project Manager Date

Appendix A Test Results obtained with Purple Card

Many important electronics test results have been obtained with the 1st and 2nd purple card prototype. The fact that both purple card prototypes worked satisfactory helped the project to stay on schedule.

- Hybrid Tests (A. Nomerotski)
- Hybrid Irradiation Tests (E. von Toerne)
- Layer 0 Noise Tests (K. Hanagaki)
- SVX4 Yield Tests (S. Lager)
- Laser Tests (G. Otero y Garzon)

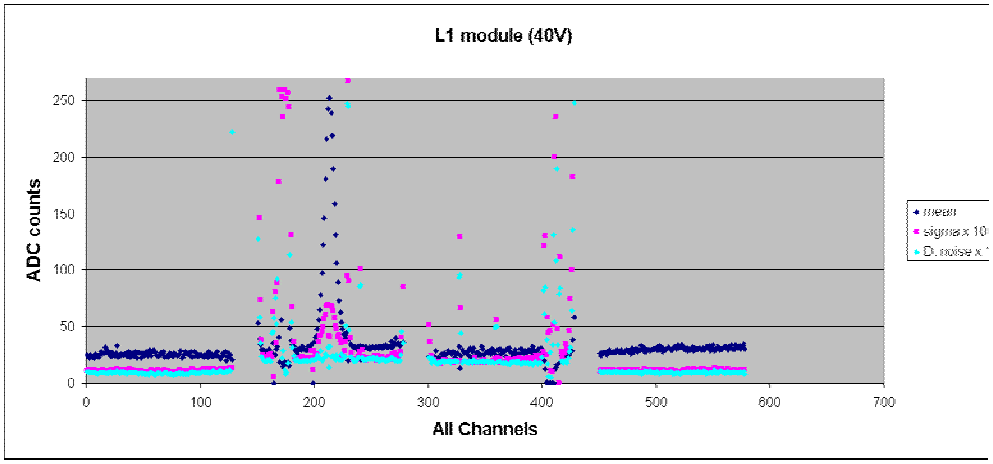

Fig 1: Laser test results with Purple Card. Signals induced by the laser pulse are located around readout channel #210.

The laser test is very close to the real operation of the electronics and verifies that the sensor/electronics combo produces physics results.

Failures of the 2nd prototype are limited to infant failures of parts on a few cards. We recommend to continue the practice that purple cards are tested for functionality at KSU, are powered over an extended period of time at Fermilab (for this a large sequencer array is available at Fermilab) and that any failures of cards are repaired and investigated at KSU.

While the first prototype had several design changes, the 2nd prototype had none. We recommend to consider the 12 2nd-prototype cards as being production cards, and to add an additional safety margin of 7 more cards to the total number. This means that the procurements will be for
75 – 12 + 7 = 70 cards.

Appendix B Pictures of the Purple Card

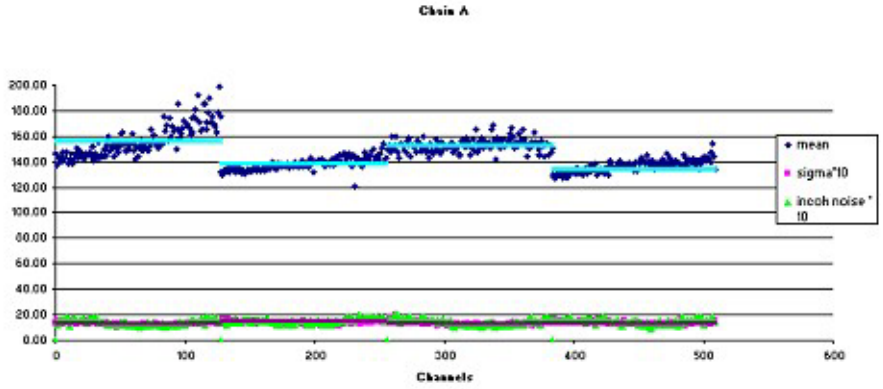

Fig. 1 Test Readout of a 4-chip hybrid with the purple card

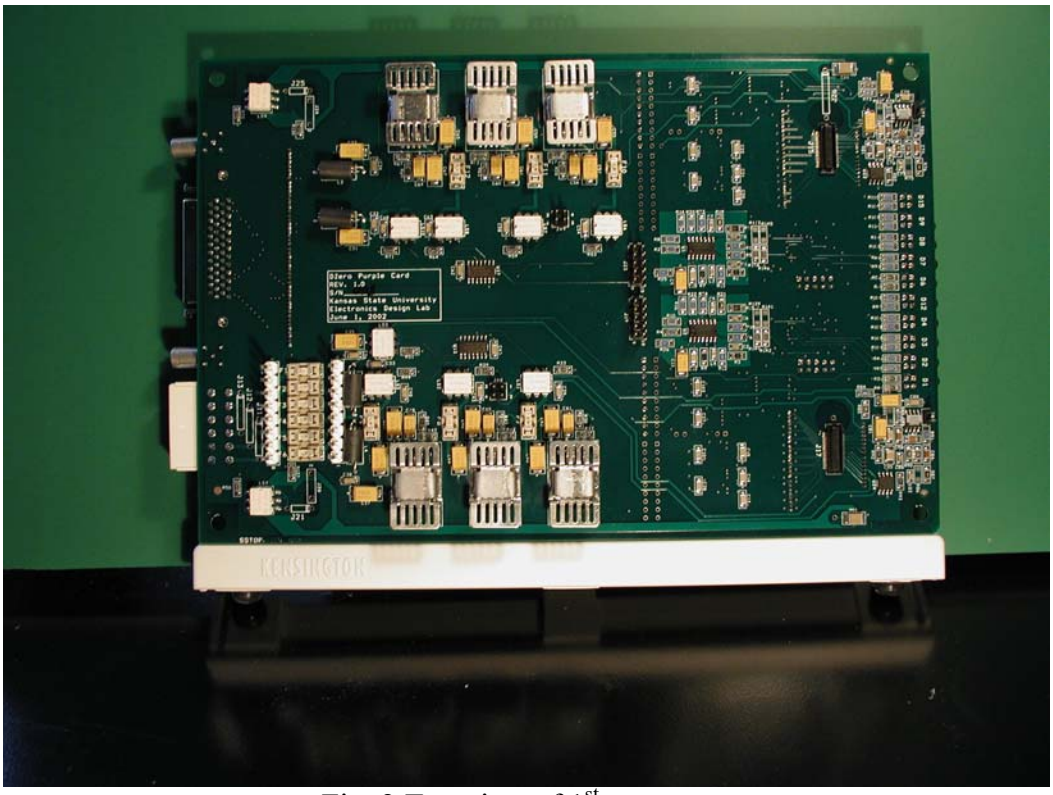

Fig. 2 Top view of 1st prototype

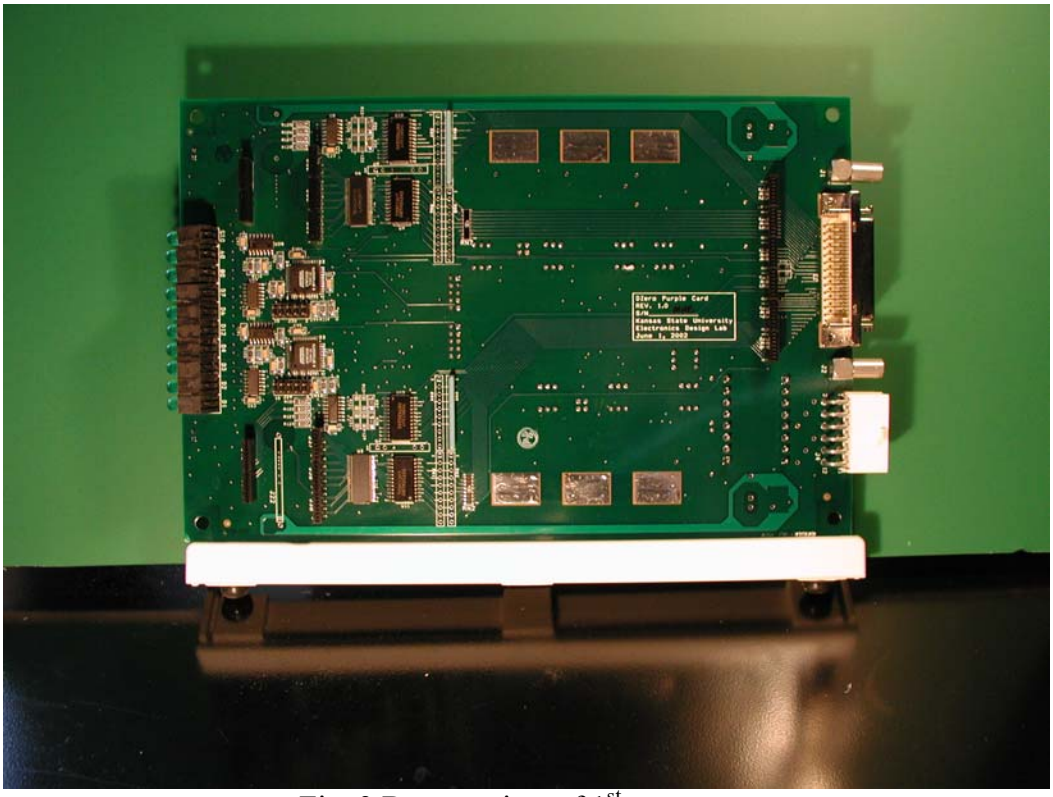

Fig. 3 Bottom view of 1st prototype

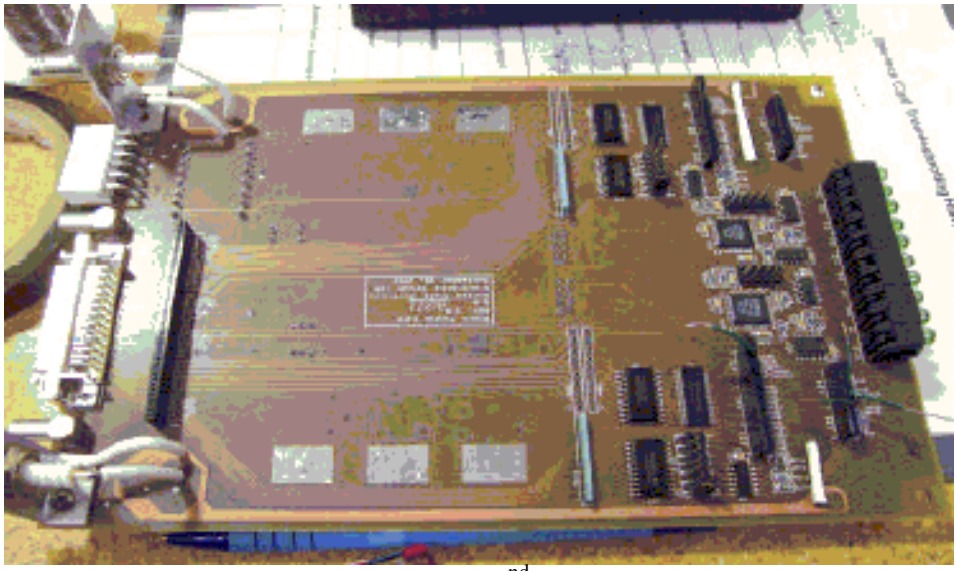

Fig. 4 View of 2nd prototype

Appendix C Specifications for the Purple Card

Test Card (WBS 1.1.2.5), aka "Purple Card" (R Sidwell, T Sobering, et al.)

08 Feb '02

This card will be used in test stands for testing and burn-in of hybrids and detectors. It buffers and translates signals between the stand-alone sequencer (SASEQ), a two-channel 6U version of the sequencer module that uses TTL logic, and the SVX4 using 2.5v differential logic. A similar module was built by KSU for run 2a teststands. The card, also known as the Purple Card, will be 6U sized or smaller and will have a connector for a 50-conductor cables from a SASEQ, and two output AVX connectors for jumper cables. Functionally the purple card is similar to the active adapter card, but with additional functions mentioned below and marked with an *. Every effort will be made to make it difficult for inexperienced operators to damage or destroy hybrids and detectors.

Agreed upon functionality (based on telephone meeting 1/8/02 of Gerber, Reay and Sidwell), and as amended by Nomerotski on 14 Jan, and KSU on 18 Jan):

1) Two channels per printed circuit board.

2) Size width 6", length TDB, location between SVX modules (per Leflat's drawing).

3) Voltage regulation of SVX4 power (and possibly board power if needed). SVX4 voltage controlled by HDI enable/disable. Power could be supplied via an 8-pin header. LEDs will indicate power status (on if LED is lit). Voltage regulator will be variable voltage version of ON regulator (part # CS5253B-1). Test points will be supplied to allow check of output voltages via well-shielded high impedance oscilloscope leads or DVM.

4) Temperature monitor (4-pin header): DC voltage out covering range -20 to 50 degrees centigrade. The target device is VMIC VMIVME3113 ADC, provides 8-bit digitization, and 64 inputs. Full range coverage is NOT mandatory. A temperature measurement of $+-2^0C$ is adequate. Assumed temperature measuring device is 1000Ω platinum RTD used in Run2a. Full range of Vout will be 0-1v, so that x10 gain mode of VMIC ADC will need to be used. Vout= 50mV will correspond to –20 degrees, Vout=+1V to +50 degrees.

⇒* 5) HV (silicon bias) supplied via a SHV connector, and controlled by HDI enable/disable from the SASEQ (300V max.). HV is passed thru to the digital jumper cable. Provision will be made for 1kV bias path with jumpers to select between 0-300V switched bias and 1kV bias. No switching will be provided for 1kV.

6) CAL-SR: two LEMO connectors ***(question: are two connectors required?)***

⇒* 7) fuses on SVX4 power, and board power. KSU will use board sockets for small cartridge type fuses. Preferred location for fuses is along the back of the board where power enters the card.

* 8) Dvalid delay provision; SIP

* 9) clock conversion from TTL to low-voltage differential

* 10) one input 50-conductor connector from SASEQ or sequencer

* 11) two pairs of output connectors- digital jumper. (twisted pair option removed)

12) One power connector will be provided with separate SVX power for each channel (pre-regulator AVDD_A, DVDD_A, AVDD_B, DVDD_B, nominally 4-5V each) with provision for jumpering these supplies on the board. Connector will also supply board power (nominally 5V) and analog (+12V) for temperature monitor. With returns, 12 pins will be required (depending on current handling capability). Connector is TBD. (Question: is it necessary/desirable to also double board power and analog to keep the channels completely isolated?)

Target date: July '02 for working prototype.
Schedule:

Feb 15 draft schematic
March 15 final schematic
May 1 final layout
June 15 first untested prototypes

Probable cost: as specified in KSU MOU.

Changes and remarks:

1) Dropped twisted pair connectors.
2) Changes since 9 Jan marked in red.
3) Resettable fuses require up to 2 sec to turn off- these are not viable in our opinion.
4) Should we put out SVX4 voltages on a header to be read out via twist and flat cable? We would prefer NOT to do this: provides an 8-10 antenna to pick up noise. However test points to probe voltages via DVM or oscilloscope will be provided. (I think the answer is "no" to remote monitoring, but I want to make sure the issue is closed. Testpoints on the board are no problem.)
5) Do we need to protect against scenarios where e.g. the DVDD line has blown a fuse, but AVDD and the transceiver power are still enabled?
6) Why is a 2" clear zone provided for behind the AVX connector on Leflat's drawing?